REMARKS

Claim 17 has been added. Claim 17 corresponds to previously cancelled claim 11, and no new subject matter has been added.

The Examiner has rejected claims 3, 5, and 6 under 35 U.S.C. 103(a) as being unpatentable over U.S. 6,232,848 issued to Manku in view of U.S. 6,813,485 issued to Sorrels and U.S. 6,522,195 issued to Watanabe.

The present invention consists of two single-transistor transconductors with a floating voltage source used to shift the relative biasing of the two single-transistor transconductors in order to implement a new, high linearity transconductance amplifier.

Manku teaches a low-voltage technique to implement RF circuits based on capacitive coupling and resonant circuits. Manku does not in any way teach improvement of linearity as described and claimed in the present application.

Sorrels teaches a transmission-gate (complementary FET switch), and discusses the linearity of Rds (switch on-resistance) versus voltage across the switch, and does not address the improvement of linearity of the type addressed by the present invention.

Watanabe teaches a low noise amplifier, but does not address linearity of the transconductance amplifier.

Attached to this response is a copy of a paper authored by the present inventors and published June 12, 2006. The paper may assist the Examiner in understanding the irrelevancy of Watanabe and Sorrels towards the present invention.

Claim 3 recites a high linearity mixer including a RF transconductance amplifier having a floating voltage source. The Examiner cites Figure 2 of Watanabe as teaching this element. However, the voltage Vcc referred to by the Examiner is not a floating voltage source, but rather is the power supply of the circuit as explained at lines 21 to 23 of column 2 of Watanabe.

Claim 3 also includes a capacitive feed-forward path within the RF transconductance amplifier. The Examiner cites the capacitor 38 and a feed forward path of Figure 2 of Watanabe as teaching this element. However, what is referred to by the Examiner as a feed forward path, element 22 in Figure 1, is a path to bypass the main

circuit. The role of the capacitor 38 is to keep the transistors 24 and 26 of Figure 1 within their linear region of operation, as explained at lines 23 to 26 of column 2. What the Examiner refers to as the capacitive feed-forward path is the combination of block 22 in Figure 1 and the capacitor 38, which is simply a bypass circuit for the main circuit.

Claim 3 also includes the limitation that the transconductance amplifier has a constant transconductance over a wide range of input differential voltages, resulting in high linearity in terms of both IIP2 and IIP3. The Examiner cites Section 6.7.4 (column 86) of Sorrels as teaching this limitation. However, as explained above, the linearity discussed by Sorrels is the linearity of Rds (switch on-resistance) versus voltage across the switch. This is not the same as providing a constant transductance in an RF transconductance amplifier over a wide range of input differential voltages.

Manku, Sorrels, and Watanabe, do not teach each and every element of claim 3, either individually or in combination. The Applicant therefore respectfully submits that a *prima facie* case of obviousness has not been established against claim 3.

Claim 5 includes all the limitations of claim 3, and further includes that the floating voltage source in the RF transconductance amplifier allows the low voltage operation of the RF transconductance amplifier. The Examiner cites Watanabe as teaching this element, but does not provide any details of where this element is taught by Watanabe. As explained above with reference to claim 3, the voltage Vcc of Watanabe is actually the power supply of Watanabe's circuit, and is not a floating voltage source within a transconductance amplifier. Manku, Sorrels, and Watanabe, do not teach each and every element of claim 5, either individually or in combination, including the limitations of claim 3 on which claim 5 is dependent. The Applicant therefore respectfully submits that a *prima facie* case of obviousness has not been established against claim 5.

Claim 6 includes all the limitations of claim 3, and further includes that the RF transconductance amplifier is self-biased and does not require any additional biasing circuitry. The Examiner cites Manku as teaching this element, but does not provide any details of where this element is taught by Manku. Manku invention discloses a low voltage technique for RF circuits based on using capacitive coupling and resonant

circuits, but makes no mention of any transconductor being self-biased. Manku, Sorrels, and Watanabe, do not teach each and every element of claim 6, either individually or in combination, including the limitations of claim 3 on which claim 6 is dependent. The Applicant therefore respectfully submits that a *prima facie* case of obviousness has not been established against claim 6.

The Examiner has rejected claim 4 under 35 U.S.C. 103(a) as being unpatentable over Manku in view of Sorrels and Watanabe and U.S. 5,529,046 issued to Werner. Claim 4 includes all the limitations of claim 3, and further includes the limitation wherein a body-effect of the p-channel single transistor transconductor and of the n-channel single transistor transconductor is eliminated to improve the linearity by obviating the threshold-voltage-modulation assisted nonlinearity. The Examiner cites Werner as teaching this element. While Werner does teach the body-effect elimination to improve linearity, Werner discusses high-voltage power MOS devices capable of 1200V. These devices are completely different in behaviour and structure from 0.18μm CMOS technology. What is true for high voltage MOS devices is not necessarily true for low-voltage devices. The Applicant respectfully submits that Werner cannot be taken to teach the limitation of claim 4 as the type of device about which Werner teaches is completely different from the type of devices recited by claim 4. Furthermore, as discussed above with reference to claim 3, none of Manku, Sorrels, Watanabe teach the remaining elements of claim 3, nor has the Examiner shown where these remaining elements are taught by Werner. For these reasons, the Applicant respectfully submits that a *prima facie* case of obviousness has not been established against claim 4.

The Examiner has rejected claim 7 under 35 U.S.C. 103(a) as being unpatentable over Manku in view of Sorrels and Watanabe and U.S. 5,721,500 issued to Karanicolas. Claim 7 is dependent on claim 3 and includes all of the limitations of claim 3. As discussed above, none of Manku, Sorrels, and Watanabe, either independently or in combination, teach each and every element of claim 3 and hence of claim 7. The Examiner has also not shown where Karanicolas teaches the elements of claim 3. The Applicant therefore respectfully submits that a *prima facie* case of obviousness has not been established against claim 7.

The Examiner has rejected claim 8 under 35 U.S.C. 102(e) as being anticipated by Manku. Claim 8 is directed to a high linearity, low power, low voltage active mixer wherein ac-coupling between an RF transconductance amplifier and a mixing stage blocks flicker noise associated with the RF transconductance amplifier. The Examiner has not indicated where this feature is taught by Manku. Manku is cited as a reference in the Background of the present application. While Manku discusses the use of capacitive coupling in order to achieve low-voltage operation, Manku does not discuss, directly or indirectly, the use of capacitive coupling to filter out flicker noise in mixers. Since Manku does not clearly teach each and every element of claim 8, the Applicant respectfully submits that claim 8 is not anticipated by Manku.

The Examiner has rejected claim 12 under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Manku. Claim 12 recites an RF transconductance amplifier which includes a p-channel single transistor transconductor. The Examiner has cited element 66 of Wanatabe as teaching this element. However, transistor 66 of Watanabe is not a p-channel single transistor transconductor, but rather is a switch controlled by digital signal denoted as "bypass" in Figure 2. Transistor 66 is not a transconductor.

Claim 12 also includes a capacitive feed-forward path within the RF transconductor amplifier. The Examiner has cited element 38 of Watanabe as teaching this element. However, capacitor 38 has nothing to do with the feed-forward capacitor as recited in claim 12. The capacitor 38 is used to keep transistors 24 and 26 within their linear mode of operation. The capacitor 38 and the circuit denoted as block 22 in Watanabe serve merely to bypass the main circuit.

Claim 12 also includes a floating voltage source. The Examiner has cited element Vcc of Watanabe as teaching this element. However, as explained at lines 21 to 23 of column 2 of Watanabe, element Vcc is not a floating voltage source but rather is the power supply of the circuit.

Since Watanabe and Manku do not teach each and every element of claim 12, either independently or in combination, the Applicant respectfully submits that a *prima facie* case of obviousness has not been established against claim 12.

The Examiner has rejected claims 13-15 under 35 U.S.C. 103(a) as being unpatentable over Watanabe in view of Manku and Werner.

Claim 13 includes all the limitations of claim 12, and further includes the limitation wherein a body-effect of the p-channel single transistor transconductor and of the n-channel single transistor transconductor is eliminated to improve the linearity by obviating the threshold-voltage-modulation assisted nonlinearity. The Examiner cites Werner as teaching this element. While Werner does teach the body-effect elimination to improve linearity, Werner discusses high-voltage power MOS devices capable of 1200V. These devices are completely different in behaviour and structure from 0.18μm CMOS technology. What is true for high voltage MOS devices is not necessarily true for low-voltage devices. The Applicant respectfully submits that Werner cannot be taken to teach the limitation of claim 13 as the type of device about which Werner teaches is completely different from the type of devices recited by claim 13. Furthermore, as discussed above with reference to claim 12, none of Manku, Sorrels, Watanabe teach the remaining elements of claim 12, nor has the Examiner shown where these remaining elements are taught by Werner. For these reasons, the Applicant respectfully submits that a *prima facie* case of obviousness has not been established against claim 13.

Claim 14 includes all the limitations of claim 12, and further includes that the RF transconductance amplifier is self-biased and does not require any additional biasing circuitry. The Examiner cites Manku as teaching this element, but does not provide any details of where this element is taught by Manku. Manku invention discloses a low voltage technique for RF circuits based on using capacitive coupling and resonant circuits, but makes no mention of any transconductor being self-biased. Manku, Sorrels, and Watanabe, do not teach each and every element of claim 14, either individually or in combination, including the limitations of claim 12 on which claim 14 is dependent. The Applicant therefore respectfully submits that a *prima facie* case of obviousness has not been established against claim 14.

Claim 15 is dependent on claim 12 and includes the same limitations discussed above which are not taught by Watanabe, Manku, and Werner, either independently or in combination. Since it has not been shown where each and every element of claim 15 is taught by the cited references, the Applicant respectfully submits that a *prima facie* case of obviousness has not been established against claim 15.

In addition, claim 17 has been added. Claim 17 corresponds to previously cancelled claim 11, although the claim has been rewritten in independent form so as to include all the limitations of previous claim 1. The Examiner had previously rejected the claim as being obvious in view of Manku and Sorrels.

Claim 17 includes the limitation that the transconductance amplifier has a constant transconductance over a wide range of input differential voltages. In rejecting previous claim 1, the Examiner cited Manku as teaching this limitation without providing any details as to where this element was taught. As discussed above, Manku is concerned with providing a low voltage technique to implement RF circuits based on capacitive coupling and resonant circuits. Manku does not in any way teach improvement of linearity as described and claimed in the present application.

Claim 17 also includes the limitation that excellent linearity (IIP2, IIP3) results, rendering the mixer suitable for a direct conversion receiver. In rejecting previous claim 11, the Examiner cited Section 6.7.4 (column 86) of Sorrels as teaching this limitation. However, as explained above, the linearity discussed by Sorrels is the linearity of Rds (switch on-resistance) versus voltage across the switch. This is not the same as providing a constant transductance in an RF transconductance amplifier over a wide range of input differential voltages.

For these reasons, the Applicant respectfully submits that a *prima facie* case of obviousness cannot be established against new claim 17 in view of Manku and Sorrels.

In view of the foregoing, it is believed that the claims as amended herein are in condition for allowance. Reconsideration and action to this end is respectfully requested.

Respectfully submitted,

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8 GHz 1V, CMOS quadrature downconverter for wireless applications

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Abstract The design and implementation of an 8 GHz CMOS quadrature downconverter, achieving simultaneously low voltage supply operation and good linearity is presented in this paper. This is achieved by relaxing the inherent trade-off between power conversion gain and linearity governing all active mixers and implementing a mixer using a new version of the bias-offset technique. The quadrature generator uses active inductors embodied in the LO buffer, and provides easy tuning by relaxing the coupling between amplitude and phase tuning of the outputs. It also provides reduced power consumption by eliminating the buffers located between the quadrature generator and the mixers. A prototype implemented in a 0.18 μm CMOS technology occupies an area of 0.44 × 0.3 mm^2, operates from a 1V power supply and features an IIP3 of +3.5 dBm, an IIP2 of better than +48 dBm, an input compression point of −5.5 dBm, a power conversion gain of +6.5 dB for the mixers and a quadrature phase and amplitude matching of better than 1.5° and 1 dB respectively over a bandwidth of 100 MHz after tuning. The overall power consumption of the quadrature downconverter is 25.8 mW.

Keywords CMOS quadrature downconverter · Active inductor · Bias-offset technique · Linearity · Low voltage

1. Introduction

The downlink of cellular phones in the next generation of mobile communication systems is expected to use orthogonal frequency division multiplexing (OFDM) as the multiple access scheme and quadrature phase-shift keying (QPSK) data modulation, operating at a data rate of 100 Mbps [1, 2]. This high data rate translates into high channel bandwidth which in turn requires good RF receiver front-end linearity to accommodate the dynamic range necessary to maintain the Bit-Error-Rate (BER) of the received signal. Future generations of wireless systems are expected to be implemented using direct conversion receivers (DCR) due to their suitability for monolithic implementation and relative ease of design for OFDM multiple access systems [3–5]. The later feature is due to the fact that by leaving the OFDM subcarriers located at DC and near DC empty[1] [6], *ac-coupling* can be used at the output of the mixer to eliminate the DC-offset and most of the flicker noise power without affecting the BER of the received signal. In a DCR, designed for future mobile phones, the quadrature downconverter must provide good linearity and low-voltage capability while maintaining small form factor and design simplicity [7, 8].

This paper presents the design and implementation of a quadrature downconverter providing good linearity at a supply voltage of 1V. It is implemented in a 0.18 μm CMOS technology and operates at 8 GHz.

2. Quadrature downconverter

The schematic of a DCR is illustrated in Fig. 1. Its RF front-end consists of three main blocks, namely a filter to eliminate the undesired frequency content of the signal and to select the channel of interest, a low-noise

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[1] As implemented in IEEE 802.11a standard for wireless local area networks (WLAN) [6].

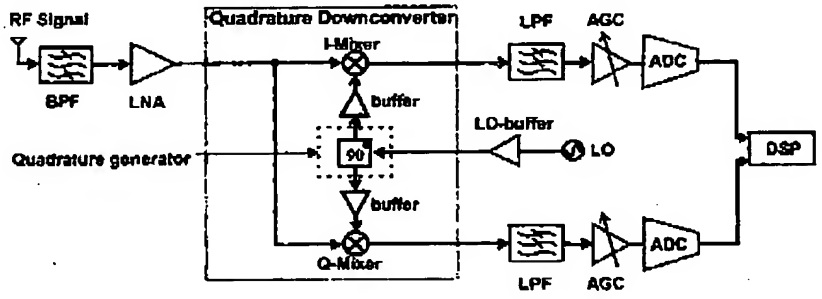


Fig. 1 Direct conversion receiver architecture

amplifier (LNA), and a quadrature downconverter to demodulate the incoming angle-modulated data. The RF signal captured by the antenna reaches the mixers after one step of amplification by the LNA. This imposes demanding requirements on the dynamic range of the mixers [7].

Quadrature signal generation from the differential local oscillator signal is an essential part of a quadrature downconverter providing the In-phase (I) and Quadrature (Q) signals. If the amplitude of the I and Q signals are not equal and/or their phase difference deviates from 90°, the error rate in detecting the baseband signal increases [4].

If the receiver is to be implemented on a single chip, the integration of the RF, analog and digital signal processing sections must all be implemented in CMOS [9]. For a tentative frequency band centered around 8 GHz [1], 0.18 μm CMOS technology is an appropriate choice for the implementation of the receiver and associated quadrature downconverter.

3. Mixer

3.1. Background

The current commutating mixer (CCM), illustrated in Fig. 2 in a block diagram form, is the most commonly used CMOS active mixer. In this architecture, the incoming RF signal is first transformed to a current by the transconductor, the signal is then downconverted to the desired IF frequency in the mixing stage. The transresistance stage is finally used to convert the IF current back to voltage.

In a conventional CCM, the mixing stage typically consists of the well known cross coupled differential pairs and the transresistance stage may be implemented using either resistors or transistors. The transconductor is commonly implemented using a simple differential pair, as illustrated in Fig. 3(a). The differential pair has a nonlinear voltage to current transfer characteristics resulting in a non-constant transconductance (G_m) as shown in Figs. 3(b) and (c) re-

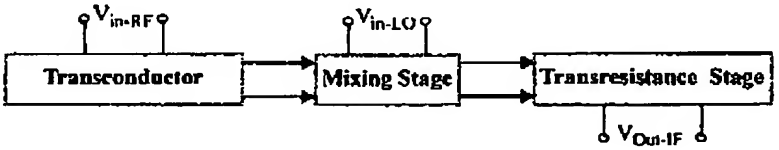


Fig. 2 CCM block diagram

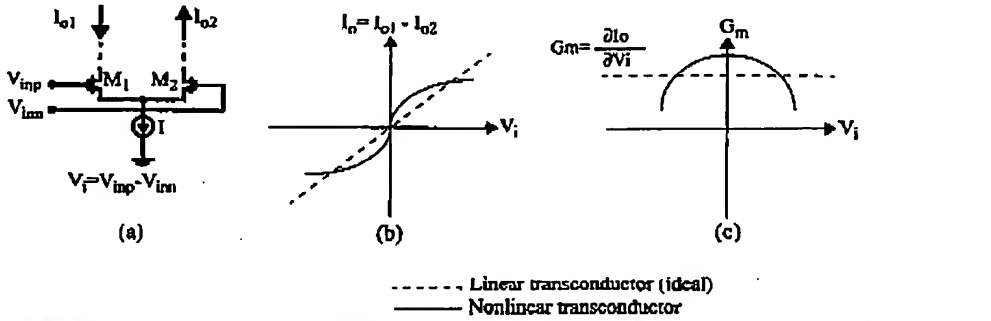


Fig. 3 Conventional transconductor used in CCM. (a) Circuit diagram, (b) Transfer characteristics, and (c) Transconductance versus input voltage

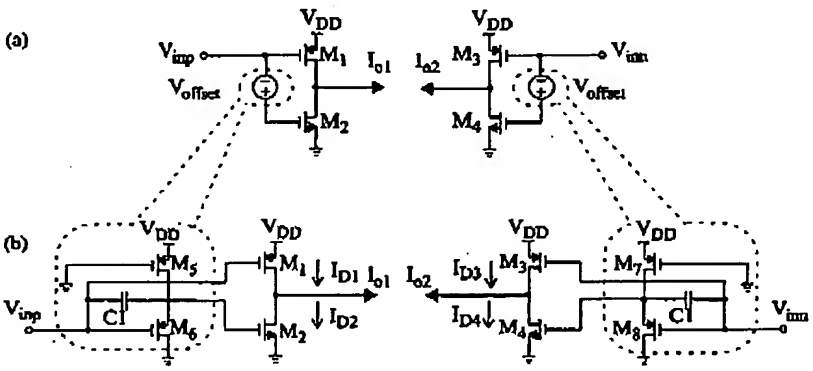


Fig. 4 The proposed transconductor for the CCM. (a) The bias offset technique for M_1 and M_2 (M_3 and M_4) using a floating voltage source. (b) The complete circuit diagram of the new differential transconductor using the bias-offset technique

spectively. This nonlinear behaviour affects the linearity of the CCM [10].

Linearization techniques applied to the CCM architecture so far either add to the complexity of the design and the power consumption [11] or include an unreasonable amount of inductive degeneration which results in a large chip area [12]. Kim et al. [13] proposed a technique to improve the linearity of RF transconductors based on harmonic-tuned multiple gate transistors which provides good linearity in terms of IIP3 (the IIP2 of the design was not reported) but has a low power conversion gain and a relatively high noise figure.

A CMOS transconductor featuring a bias-offset technique introduced by Wang and Guggenbuhl [14] demonstrated good linearity while maintaining design simplicity. The original form of the bias-offset technique applied to the conventional CMOS transconductor is not suitable for high frequency, low voltage applications.

In this work, a new version of the bias-offset technique is used in the transconductor design to relax the trade-off between the power conversion gain and linearity while preserving the gain of the circuit and operating at low supply voltages.

3.2. Mixer circuit design

Figure 4(a) illustrates the transconductor concept used in this work to improve the linearity of the CCM [15, 16]. The offset voltage V_{offset} provides a controlled bias between the gates of M_1 and M_2 (M_3 and M_4). In order to decrease the power consumption of the circuit, current reuse [17, 18] is employed in the design through the N and P-channel common source transistors M_1 and M_2 (M_3 and M_4). This technique allows doubling the transconductance gain for the same power consumption.

In order to gain analytical insight into the linearization technique applied to the transconductance stage of the mixer, the transconductance of the circuit shown in Fig. 4(a) was derived using the following I_D-V_{GS} transfer characteristics for the MOS transistors [19]

$$I_D = \frac{\mu_o C_{ox}}{2\left[1+\theta\,(V_{GS}-V_{th})+\xi\frac{V_{DS,sat}}{L}\right]}\cdot\frac{W}{L}\cdot(V_{GS}-V_{th})^2 \qquad (1)$$

where μ_0 is the low field bulk mobility of the carriers, C_{ox} is the gate oxide capacitance per unit area, θ is the mobility degradation factor due to the vertical electric field in the gate of the device, ξ is the mobility degradation factor due to the horizontal electric field in the channel of the MOS transistor, $V_{DS,sat}$ is the saturation drain-source voltage of the transistor, V_{GS} is the gate to source voltage of the device, V_{th} is the threshold voltage of the transistor and W and L are the width and the length of the device respectively. This equation preserves the required simplicity for hand calculations while taking into account short channel effects which affect the linearity of the transconductance of the device. The transconductance g_m of a MOS transistor can be calculated from (1) as follows

$$g_m = \frac{\partial I_D}{\partial V_{GS}} \approx \mu_o C_{ox}\cdot\frac{W}{L}\cdot\frac{V_{GS}-V_{th}}{1+2\left(\theta+\frac{\xi}{L}\right)\cdot(V_{GS}-V_{th})} \qquad (2)$$

The transconductance G_m of the half circuit consisting of M_1, M_2 and the floating voltage source V_{offset} in Fig. 4(a) is given by

$$G_m = \frac{\partial I_{o1}}{\partial V_{inp}} = \frac{\partial\,(I_{D1}-I_{D2})}{\partial V_{inp}} = \frac{\partial I_{D1}}{\partial V_{inp}} - \frac{\partial I_{D2}}{\partial V_{inp}} \qquad (3)$$

It is observed that $V_{SG1} = V_{DD}-V_{inp}$ and $V_{GS2} = V_{inp} + V_{offset}$, therefore for a fixed V_{DD} and V_{offset}

$$\partial V_{inp} = -\partial V_{SG1} = \partial V_{GS2} \qquad (4)$$

From Eqs. (3) and (4), G_m can be expressed in terms of the transconductances g_{m1} and g_{m2} of transistors M_1 and M_2 as

$$G_m = -(g_{m1} + g_{m2}) \tag{5}$$

From Eqs. (2) and (5), G_m can be obtained in terms of V_{offset}, V_{inp} and the aspect ratio of transistors M_1 and M_2 as

$$G_m = -C_{ox}\mu_{on}\cdot\left(\frac{W}{L}\right)_2 \cdot \frac{V_{inp}+V_{offset}-V_{thn}}{1+2\left(\theta_n+\frac{\delta_n}{L_2}\right)\left(V_{inp}+V_{offset}-V_{thn}\right)} - C_{ox}\mu_{on}\cdot\left(\frac{W}{L}\right)_1 \cdot \frac{V_{dd}-V_{inp}-|V_{thp}|}{1+2\left(\theta_p+\frac{\delta_p}{L_1}\right)\left(V_{dd}-V_{inp}-|V_{thp}|\right)} \tag{6}$$

To achieve a maximally flat (maximally constant) G_m as a function of V_{inp} at peak G_m, the second and third order derivatives of G_m with respect to V_{inp} are set to zero at peak G_m by choosing a proper value for V_{offset} and $(W/L)_2/(W/L)_1$. As shown in Fig. 4(b), the voltage V_{offset} is realized by transistors M_5 and M_6 (M_7 and M_8). It is given as a function of the aspect ratios of M_5 and M_6 (M_7 and M_8) by the following equation

$$V_{offset} = \frac{\alpha}{\alpha+1}|V_{thp}| + \sqrt{\left(\frac{\alpha}{\alpha+1}|V_{thp}|^2 - \frac{\alpha|V_{thp}|^2 - V_{dd}^2}{\alpha+1}\right)} \tag{7}$$

where

$$\alpha = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_5} \tag{8}$$

The low-voltage capability of the transconductor shown in Fig. 4(b) is achieved by offsetting the gate bias voltage of M_1 and M_2 (M_3 and M_4) to provide simultaneously high gate to source voltage for both M_1 and M_2 (M_3 and M_4) at a supply voltage of 1 V. The design ensures simultaneous operation of M_1, M_2, M_3 and M_4 in the active region over a relatively large range of the input signal levels. This feature along with the fully symmetric characteristics of the design are key to the good linearity behaviour of the design in terms of second-order nonlinearities. Capacitor C_1 in Fig. 4(b) provides a feedforward path for the RF signal and improves the high frequency performance of the floating voltage source. By introducing C_1, the RF signal appearing at the gates of M_1 and M_2 (M_3 and M_4) will be identical, as required for the proper operation of the circuit.

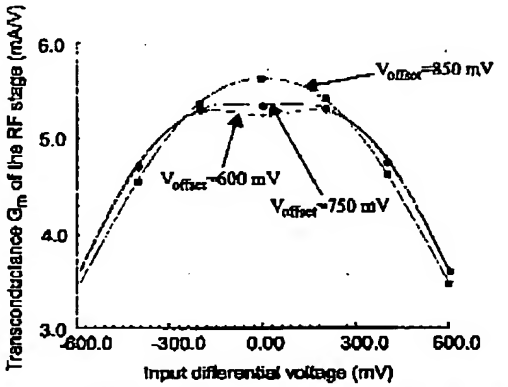


Fig. 5 Transconductance G_m of the transconductor, for three different values of the offset voltage. The flat transconductance (V_{offset} = 750 mV) was obtained for $(W/L)_1$ = 32 μm/0.18 μm, $(W/L)_2$ = 20 μm/0.18 μm, $(W/L)_5$ = 30 μm/0.25 μm, $(W/L)_6$ = 16 μm/0.18 μm

Figure 5 illustrates the simulated transconductance G_m of the half circuit shown in Fig. 4(b) and consisting of M_1, M_2, M_5 and M_6 for three different values of V_{offset} and for $(W/L)_1$ = 32 μm/0.18 μm and $(W/L)_2$ = 20 μm/0.18 μm. As observed, a value of V_{offset} = 750 mV results in a constant transconductance over a wide range of the input differential voltage, which in turn translates into good linearity performance of the mixer.

The final schematic of the mixer under consideration is illustrated in Fig. 6 and the values of all the components are given in the figure. As illustrated, the RF transconductor is ac-coupled to a mixing stage made of cross-coupled differential pairs which is terminated in a lowpass load to eliminate any undesirable high frequency content in the output signal. Active loads are avoided at the output of the mixer to minimize flicker noise and improve the NF at baseband frequencies. The cross coupled mixing stage is biased through LC resonators (set at 8 GHz) instead of the conventional current sources to enable low-voltage operation [20] and optimize the performance of the mixing stage at 8 GHz.

Table 1 summarizes the post layout simulated performance of the mixer. The present design offers considerable advantages over the conventional CCM [12] in terms of gain and linearity and in addition operates at 1 V supply which is not possible in the conventional case. Specifically, it relaxes the tradeoff between power conversion gain and linearity of CCMs which allows for simultaneously improving the gain and linearity of the mixer.

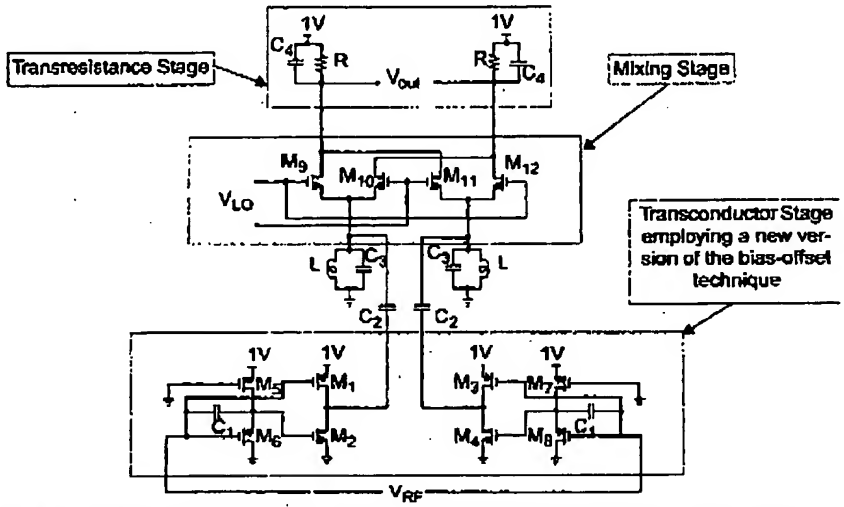


Fig. 6 Schematic of the Proposed Mixer. (M_1, M_3: 32/0.18; M_2, M_4: 20/0.18; M_5, M_7: 30/0.25; M_6, M_8: 16/0.18; M_9, M_{10}, M_{11}, M_{12}: 8/0.18; all dimensions are in microns. L = 0.5 nH; C_1 = 1pF, C_2 = 8pF, C_3 = 0.8 pF, C_4 = 2pF, R = 500 Ω). The DC level of the RF input is 0 V and the DC value of the LO input is 0.55 V

Table 2 shows the effect of process variations on the performance of the proposed mixer architecture; note that the power worst case and speed worst case listed in the table, include a power supply variation of +10% and −10% respectively to fully account for the worst case condition. The table illustrates the relative robustness of the design for process and supply voltage variation.

4. Quadrature generator

Quadrature generators reported in the literature so far fall within one of the following categories: RC-CR filters [21], polyphase filters [22], subtraction and addition [23], frequency division [24], cellular oscillator networks [25], ring oscillators [3] and quadrature LC-oscillators [26]. Most of these approaches either have a large form factor due to the use of resistors and capacitors consuming a relatively high chip area, or result in an increase in power consumption due to the requirement for RF buffers between the quadrature generator and the mixers, or due to the use of a VCO operating at twice the frequency of interest. A quadrature generator integrating the quadrature generation scheme into the LO-buffer was introduced by Steyaert and Roovers [27]. The design has a small form factor but has tendency toward causing instability due to the negative resistance present at its inputs and caused by the capacitive degeneration used to provide the 90° phase shift. In the following subsections, the design and analysis of a new quadrature generator that integrates the quadrature generation scheme into the LO-buffer using active inductors, is presented.

Table 1 Post layout simulation results

	Post layout simulation
Technology	0.18 μm CMOS, with zero-Vth nmos transistors
Supply Voltage	1 V
Frequency	8 GHz
Noise figure	11 dB
IIP3	+2 dBm
IIP2	+52 dBm
P-1dB	−10 dBm
Power conversion gain	+12 dB
Power consumption	6.2 mW

4.1. Architecture

The block diagram of the proposed design is illustrated in Fig. 7 [28]. It consists of a LO-buffer, a differential active

Table 2 Effect of process and supply voltage variations on the performance of the mixer

	Typical process parameters	Speed worst case parameters	Power worst case parameters
Gain	12 dB	10 dB	7 dB
IIP3	+2 dBm	+2.5 dBm	+4 dBm
IIP2	+52 dBm	+54 dBm	+58 dBm
P-1dB	−10 dBm	−9.5 dBm	−7.5 dBm
Power consumption	6.2 mW	6 mW	6.9 mW

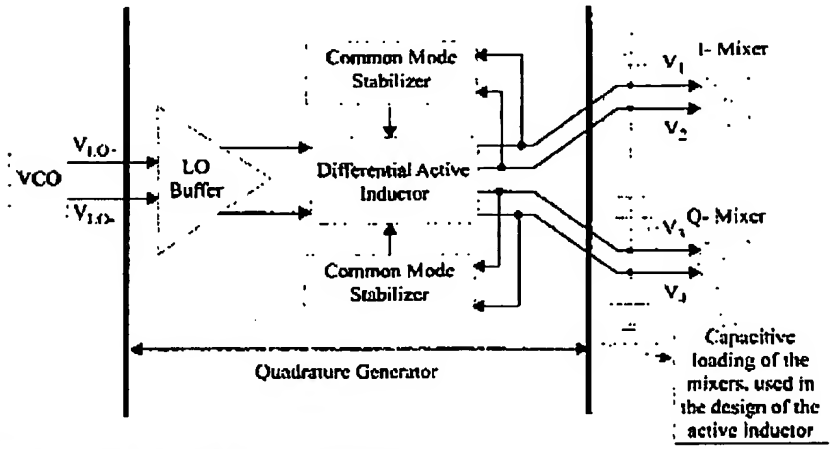


Fig. 7 Block diagram of the quadrature generator under consideration

inductor and two common-mode stabilizers. In this architecture, there is no need for isolating the quadrature generator from the mixers by using additional buffers, since the capacitive loading of the mixers on the quadrature generator can be used in the active inductor design. The LO-buffer consists of common source n-channel transistors loaded by p-channel transistors. The differential active inductor is illustrated in Fig. 8 and is based on the conventional G_m-C structure [29]. In Fig. 8, g_{mi} and g'_{mi} are the transconductances of M_7 (M_8) and M_5 (M_6) respectively.

The common-mode stabilizer, shown in Fig. 9, consists of two cross coupled transistors (M_{21}, M_{22}) and transistor M_{23} which is a zero-threshold MOS transistor and is designed to operate in the triode mode. The circuit is added to the design to stabilize the common-mode behaviour of the differential active inductor by moving its common-mode

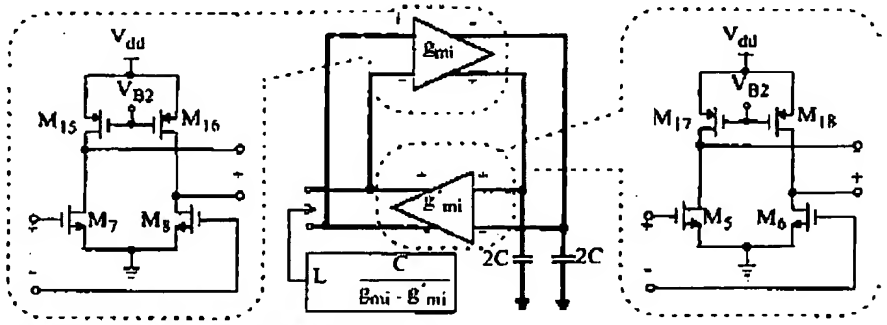
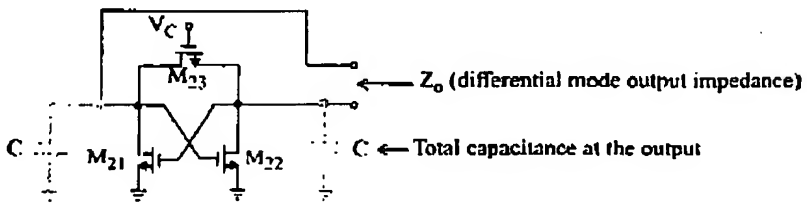


Fig. 8 Differential active inductor implementation based on the G_m-C architecture

Fig. 9 Common-mode stabilizer circuit



right-half-plane pole to the left-half-plane [30]. In the differential mode of operation, the common-mode stabilizer appears as an impedance Z_o with a real part given by

$$Re\{Z_0\} = -\frac{g_{ms}}{\omega^2 C^2 + g_{ms}^2} \Big\| r_{ds} \tag{9}$$

where, g_{ms} is the transconductance of M_{21} or M_{22}, C is the total parasitic capacitance at the outputs of the common-mode stabilizer and r_{ds} is the output resistance of M_{23} in the triode region which can be controlled by V_C.

4.2. Design and analysis

The complete circuit of the quadrature generator is shown in Fig. 10. Transistors M_1, M_2, M_{13} and M_{14} form the LO-buffer and M_3, M_4, M_{19} and M_{20} are dummy transistors identical to M_1, M_2, M_{13} and M_{14} and are added to the circuit to preserve the symmetry of the design. The capacitors C_{aux}, implemented by the gate to source and gate to drain capacitances of the n-channel transistors M_9, M_{10}, M_{11} and M_{12}, are included in the design to relax the coupling between the amplitude and phase tuning of the quadrature generator by cancelling out the gate to drain capacitance of transistors M_1, M_2 (M_3, M_4). This is done by setting the aspect ratio (W/L) of M_9 to M_{12} to be half of that of M_1 to M_4 such that the sum of the gate to drain and the gate to source capacitances of M_9 to M_{12} equals the gate to drain capacitance of M_1 to M_4. To obtain an analytical insight into the quadrature signal generation of the circuit, the outputs of the circuit of Fig. 10 were derived in terms of the differential local oscillator voltage (V_{LO}). This was done by replacing transistors M_1, M_2 and M_5 to M_8 by the small signal model illustrated in Fig. 11 and replacing transistors M3, M4 and M13 to M20 by parallel RC circuits, representing the output resistance and the sum of the

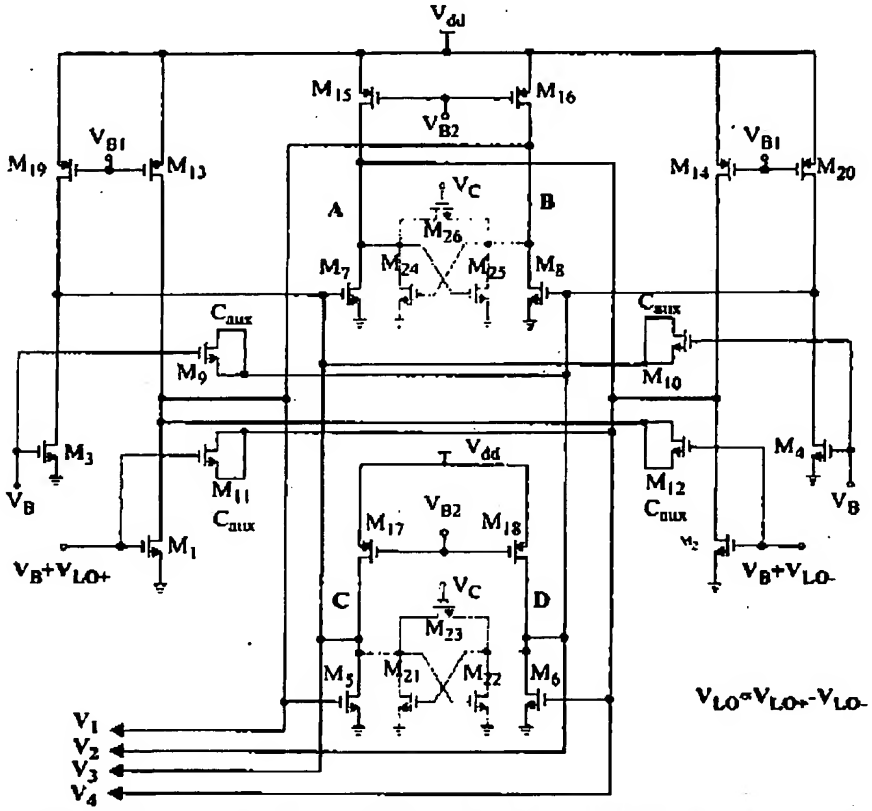


Fig. 10 Circuit of the quadrature generator. (M_1 to M_8 : 10/0.18; M_{21}, M_{22}, M_{26} and M_{25}: 9/0.18; M_{13}, M_{14}, M_{19} and M_{20} : 12/0.18; M_9 to M_{12} : 5/0.18; M_{15} to M_{18} : 12/0.18; M_{23} and M_{24} are zero threshold voltage devices: 6/0.5; all dimensions are in μm. $V_{dd} = 1$ V, $V_B = 750$ mV, $V_{B1} = 150$ mV, $V_{B2} = 0$, $V_C = 850$ mV)

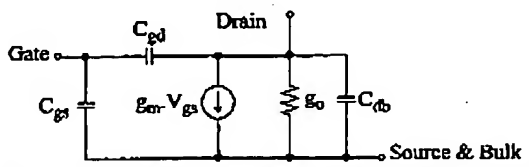


Fig. 11 Small signal model used to analyze the quadrature generator

drain to bulk and drain to gate capacitances of each transistor. In the differential mode of operation, the common-mode stabilizers were replaced by a negative resistance which was designed to cancel out the equivalent conductance at nodes A, B, C and D in Fig. 10, which is necessary for the quadrature phase generation at the outputs. The output capacitance of the common-mode stabilizer is merged in the equivalent capacitances at nodes A, B, C and D. The resulting equations specifying voltages V_1 to V_4 are listed below:

$$V_1 = H(s)[g_{mb} + s(C_{aux} - C_{gdb})] \times \left[g_{oeq} + s(2C_{gdi} + C_{gdb} + C_{eq} + C_{aux})\right] V_{LO} \quad (10)$$

$$V_2 = H(s)\left[g_{mb} + s(C_{aux} - C_{gdb})\right] g_{mi} V_{LO} \quad (11)$$

$$V_3 = -H(s)\left[g_{mb} + s(C_{aux} - C_{gdb})\right] g_{mi} V_{LO} \quad (12)$$

$$V_4 = -H(s)\left[g_{mb} + s(C_{aux} - C_{gdb})\right] \times \left[g_{oeq} + s(2C_{gdi} + C_{gdb} + C_{eq} + C_{aux})\right] V_{LO} \quad (13)$$

where C_{gdb} is the gate to drain capacitance of the n-channel transistors in the LO-buffer, C_{gdi} represents the gate to drain capacitor of the n-channel transistors forming the active inductor, C_{eq} is the equivalent capacitance at nodes A, B, C and D; g_{mb} is the transconductance of the n-channel transistors in the LO-buffer; g_{mi} is the transconductance of the n-channel transistors in the active inductor and g_{oeq} is the equivalent conductance at nodes A, B, C and D.

As is observed from Eqs. (10) to (13), by eliminating the equivalent conductance at nodes A, B, C and D in Fig. 10 (i.e. $g_{oeq} = 0$), using the negative output conductance of the common-mode stabilizer circuit, controlled by V_C, the voltages V_1 and V_4 will have 90° phase shift relative to V_2 and V_3 respectively. The 90° phase shift is represented by the term $s(2C_{gdi} + C_{gdb} + C_{eq} + C_{aux})$ in the analytical expressions for V_1 and V_4. V_C can also be used to apply an optional automatic phase tuning signal [31] to this circuit to compensate for process and temperature variations of the output phase. From (10) to (13) it is clear that once the quadrature phase matching is achieved ($g_{oeq} = 0$), the amplitudes of V_1 to V_4 can be made equal at a desired frequency, provided that

$$g_{mi} = \omega(2C_{gdi} + C_{gdb} + C_{eq} + C_{aux})$$

where ω is the desired angular frequency. The value of g_{mi} is adjusted by setting the DC currents of M_5 to M_8 using the p-channel transistor M_{15} to M_{18} in Fig. 10 to satisfy Eq. (15).

By choosing $C_{aux} = C_{gdb}$, the multiplicand $[g_{mb} + s(C_{aux} - C_{gdb})]$ in Eqs. (10) to (13), reduces to g_{mb}, and therefore the magnitudes of V_1, V_2, V_3 and V_4 can be adjusted independently of their phases by varying g_{mb}. The transconductance g_{mb} is controlled by the bias current flowing through M_1 and M_2 using the p-channel transistors M_{13} and M_{14} and V_{B1}. An optional automatic amplitude control signal V_{B1} can be applied to the gates of M_{13} and M_{14} to compensate for process and temperature variations of the output amplitudes.

Figure 12 illustrates the post layout simulated magnitude and phase behaviour of the four outputs of the quadrature generator of Fig. 10, along with the time domain behaviour of the circuit. The circuit is designed such that it has a simulated gain of 0 dB to prevent the attenuation of the local oscillator signal. As observed, the simulation results confirm the equations characterizing the outputs. The circuit exhibits a phase difference of 90° between the outputs and equal amplitude for the four quadrature outputs at 8 GHz, as shown in Fig. 12(b).

$$H(s) = \frac{(g_{mi} - 2sC_{gdi})^2 - [g_{oeq} + s(2C_{gdi} + C_{gdb} + C_{eq} + C_{aux})]^2}{[(g_{oeq} + s(2C_{gdi} + C_{gdb} + C_{eq} + C_{aux}))^2 + 2C_{gdi}(g_{gmi} - sC_{gdi})][s^2C_{gdi}^2 + (g_{gmi} - sC_{gdi})^2]^2} \quad (14)$$

5. Experimental results

The microphotograph of the fabricated quadrature downconverter implemented in a 0.18 μm CMOS technology is shown in Fig. 13. The chip area is 0.44 × 0.3 mm^2 including two mixers each occupying an area of 0.28 × 0.2 mm^2 and a quadrature generator with a silicon area of 0.15 × 0.09 mm^2. The mixers and the quadrature generator are highlighted on the micrograph. Two on-chip output buffers are integrated with the quadrature downconverter. The buffers match the output of the mixer to 50 Ω at baseband frequencies to allow for proper interfacing with the measurement setup. This is done by setting the transconductance (g_m) of the source follower stage equal to 20 mA/V (1/(50 Ω)).The RF and LO inputs of the mixer were externally matched to 50 Ω in the process of measurement using manual microwave tuners.

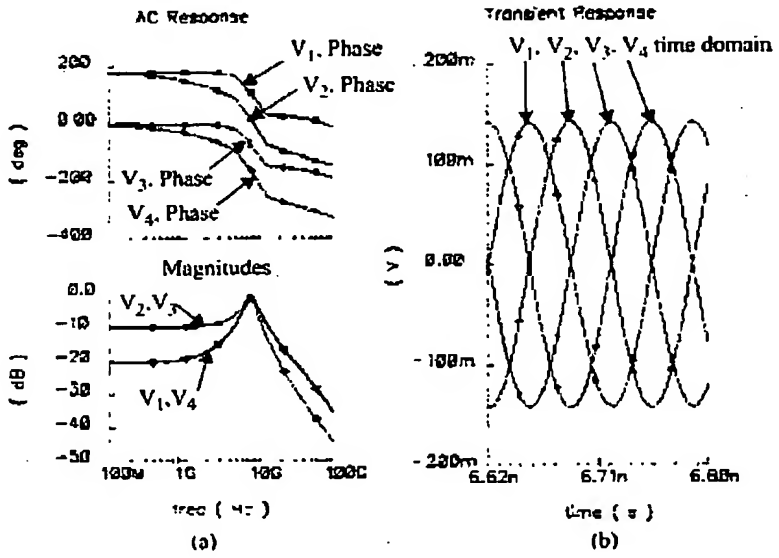


Fig. 12 Post-layout simulation characteristics of the quadrature generator. (a) The magnitude and phase of the transfer function of the four outputs. (b) The time domain quadrature outputs

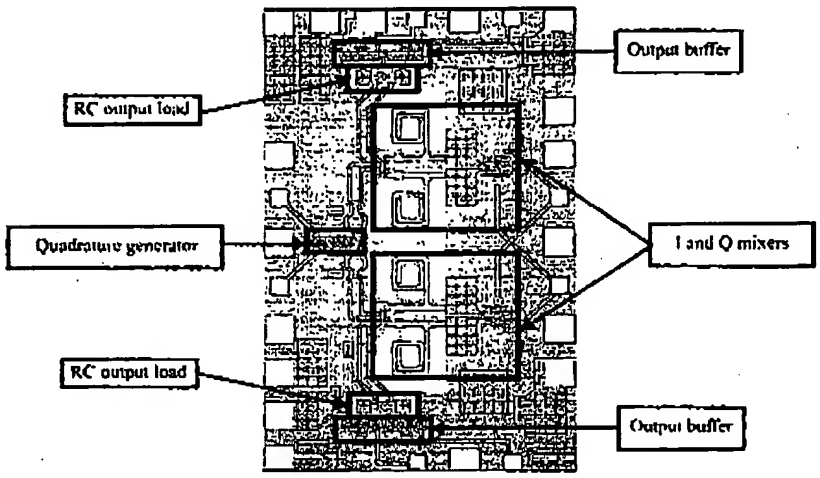


Fig. 13 Micrograph of the fabricated quadrature down-converter

Figure 14 illustrates the two-tone test results at 8001 and 8003 MHz. The intercept of the linear extrapolation of the first and third order terms indicates a measured IIP3 of +3.5 dBm. The IIP2 of the mixer was found to be better than +48 dBm. Due to the relatively high noise floor of the measurement setup, particularly the spectrum analyzer, and the fact that the magnitude of the second order nonlinearity was small and comparable to the noise floor for most values of the input signal power below the 1 dB compression point of the mixer, it was only possible to observe that the IIP2 of the mixer is better than +48 dBm. The corresponding simulated results for IIP3 and IIP2 were +2 dBm +52 dBm respectively.

Figure 15 shows a plot of the power transfer characteristics of the mixer. From the plot, it is apparent that the mixer exhibits a 1-dB compression point of −5.5 dBm and a power conversion gain of +6.5 dB. By comparison, the simulated power conversion gain and the 1-dB compression point are +12 and −10 dBm respectively. The lower values of the measured power conversion gain (PCG) is partly due to the

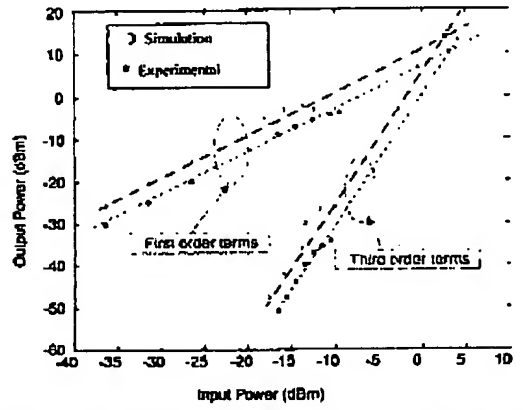


Fig. 14 Two-tone test revealing a measured IIP3 of +3.5 dBm and a simulated IIP3 of +2.5 dBm

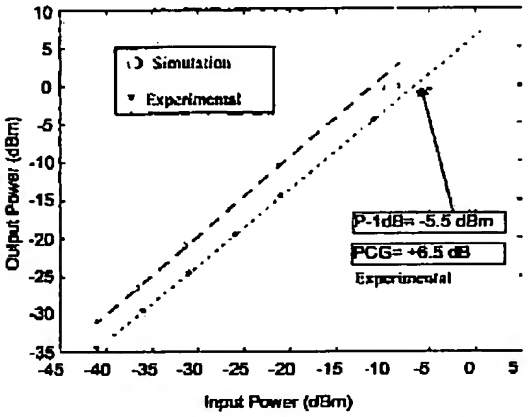


Fig. 15 Power transfer characteristics of the mixer illustrating a measured 1-dB compression point of −5.5 dBm and a power conversion gain (PCG) of +6.5 dB versus a simulated P-1 dB of −9.5 dBm and a PCG of +10 dB

de-tuning of the LC resonator, and the parasitic resistances at the RF signal path which are not extracted by the design kit used in this work.

The mixer exhibits a RF to LO isolation of 60 dB at 8 GHz. This is achieved by maximizing the separation of the RF and the LO sections of the mixer to minimize the substrate assisted coupling between the two ports and by placing the transistors of the mixing stage individually in deep N-wells isolated from the substrate. The mixer exhibits a relatively low noise figure of 11 dB at baseband frequencies.

Figure 16 shows the measured and simulated quadrature phase and amplitude matching of the outputs of the circuit for a peak-to-peak differential local oscillator input of 300 mV (measured output of 250 mV peak-to peak at the output of the quadrature generator which results in a gain of roughly −2 dB) over a bandwidth of 100 MHz which is the tentative targeted bandwidth for the future generation of mobile phones. The circuit demonstrates a measured quadrature phase and amplitude matching of better than 1.5° and 1 dB over the bandwidth of interest. The fine tuning of the quadrature generator performance requires applying a variation of less than 150 mV in V_C (4° of variance in the output quadrature phase) and less than 80 mV in V_{B1} (1 dB of variance in amplitude) to achieve the values reported in Fig. 16. These control voltage variations can be generated by automatic amplitude and phase tuning circuitry previously reported in the literature [31]. The simulation results for the effect of process and supply voltage variations (10%) on the performance of the design reveal a phase and amplitude variations of 6° and 1 dB respectively which can be easily tuned using the amplitude and phase control voltages.

Figure 17 illustrates the measured time domain representation of the outputs of the quadrature generator. The experimental gain of the quadrature generator at 8 GHz is almost 2 dB lower than the simulated value. The slight discrepancy between the experimental and simulation is partly attributed to the uncertainty in measurements due to the built-in jitter of the equipment.

The measured characteristics of the quadrature downconverter are listed in Table 3. Post-layout simulation results are also listed in the table for the sake of comparison. *This is the first reported CMOS quadrature downconverter operat-*

Table 3 Experimental characteristics and post-layout simulation results of the mixer and the quadrature generator

Circuit	Parameter	Experimental	Post-layout simulation
Mixer	Supply Voltage	1 V	1 V
	RF & LO frequency	8 GHz	8 GHz
	Conversion Gain	+6.5 dB	+12 dB
	IIP2	>+48 dB	+52 dBm
	IIP3	+3.5 dB	+2 dBm
	P-1dB	−5.5 dBm	−10 dBm
	LO-RF Isolation	60 dB	–***
	Noise figure (white)	11 dB	11 dB
	Power consumption	6.9 mW	6.2 mW
	Core chip area	0.28×0.2 mm²	–
Quadrature generator	Supply voltage	1 V	1 V
	I/*Q* gain mismatch*	<1 dB	<0.3 dB
	I/*Q* phase mismatch*	<1.5°	<1°
	Power consumption**	12 mW	12 mW
	Core chip area	0.1 5×0.09 mm²	–

*Over a bandwidth of 100 MHz.

**Including the LO-buffer.

***Since part of the LO-RF isolation degradation is substrate-assisted, only the measured result is relevant, since in the design kit under consideration, substrate models were not available.

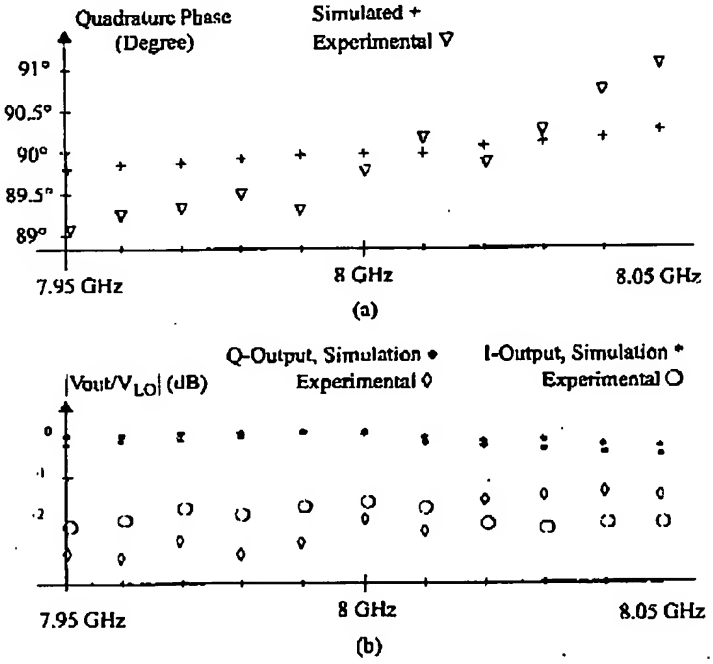


Fig. 16 Comparison between measurement and simulation results. (a) Quadrature phase. (b) Magnitude of the transfer function of the outputs

ing in the 8 GHz band. The design features relatively high power conversion gain and linearity at 1 V supply voltage due to the new bias-offset technique applied to the mixer transconductor stage.

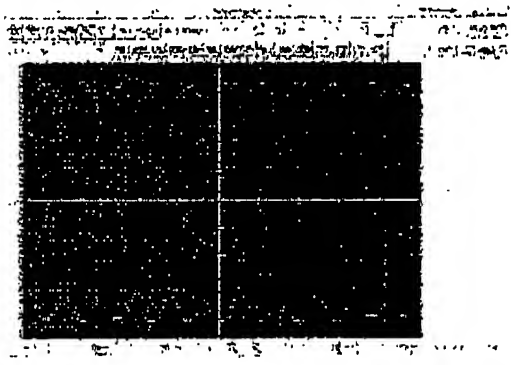


Fig. 17 The time domain measured output of the quadrature generator

6. Conclusion

The design and implementation of the first reported 8 GHz CMOS quadrature downconverter operating from a 1 V power supply and suited for direct conversion receivers was presented in this paper. It is implemented in the CMOS 0.18 μm technology. The quadrature downconverter occupies a silicon area of 0.44 × 0.26 mm^2 and consumes 25.8 mW. The mixers employ a new version of the bias-offset technique to achieve low operating supply voltage and good linearity at a reasonable power conversion gain. The mixers require a LO power of −3 dBm, and feature an IIP2 better than +48 dBm, an IIP3 of +3.5 dBm, a power conversion gain of +6.5 dB, a P-1 dB of −5.5 dBm and good isolation of 60 dB between the RF and the LO ports. The quadrature generator uses active inductors in the LO-buffer for quadrature generation. The circuit relaxes the coupling between the amplitude and quadrature phase tuning which makes it easier to apply automatic tuning circuitry to the design to compensate for process and supply voltage variations. It eliminates the need for buffering stages to isolate the quadrature generator from the mixers which in turn results in a considerable reduction in power consumption. It features a quadrature amplitude and phase matching of bet-

ter than 1.5° and 1 dB respectively over a bandwidth of 100 MHz.

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Dr. Salama is a Fellow of the Institute of Electrical and Electronics Engineers, a Fellow of the Royal Society of Canada, a Fellow of the Canadian Academy of Engineering, a member of the Association of Professional Engineers of Ontario, the Electrochemical Society and the Innovation Management Association of Canada.